PREVENTING DIELECTRIC THICKENING OVER A GATE AREA OF A TRANSISTOR

ABSTRACT OF THE INVENTION

A process for a memory transistor (e.g. flash-EEPROM cell), which includes forming an isolation-spacer between a control gate and an erase line over a floating gate by first growing a thin thermal oxide to be in contact with the first sidewall of control gate and thereafter depositing fluorinated-TEOS or tetramethylsilane (TMS) based LPCVD oxide at low temperature of about 250 degrees centigrade. The choice of deposited oxide have lower dielectric constant than that of thermal silicon dioxide which lowers the parasitic capacitance between word lines and erase lines and thereby increases speed performance. The process can be used to form low-K (low dielectric constant) dielectric insulation between word lines of in all types of memory chips including DRAM and Flash NVM.

The process prevents the formation of a poly-oxide beak under the control gate, thereby the first insulator between the control gate and the floating gate has a uniform thickness.

The transistor programs efficiently, is reliable, has low manufacture cost and is physically and electrically down scalable.